REMARKS

I. TITLE

The title has been amended per the examiner's requirement to be more clearly indicative of the invention, and now reads "APPARATUS AND METHOD FOR SEPARATE ASYMMETRIC CONTROL PROCESSING AND DATA PATH PROCESSING IN A DUAL PATH PROCESSOR."

II. CLAIMS 19 AND 21, STATUTORY SUBJECT MATTER 35 U.S.C. § 101

Claims 19 and 21 stand rejected under 35 U.S.C. § 101 as allegedly directed to non-statutory subject matter because the term "program code means" purportedly could include written code.

The preambles of claims 19 and 21 each originally stated the term "A computer program product comprising program code means which include a sequence of instruction packets." To clarify the wording, the preambles of claims 19 and 21 are amended to recite "computer-readable medium comprising a sequence of instruction packets." See MPEP § 2106(IV)(B)(2)(a) for additional discussion regarding statutory product claims.

III. CLAIMS 1-20, INDEFINITENESS 35 U.S.C. § 112

Claims 1-20 stand rejected as allegedly indefinite due to the terms "relatively narrower" and "relatively wider." Independent claims 1, and 18-20 have been amended to delete said terms and clarify the claimed width. For example, the terms "a first bit width" and "a second bit width wider than the first bit width" are now used in claim 1. Thus, claims 1-20 are not indefinite after the amendments.

IV. CLAIMS 1-21, PRIOR ART REJECTIONS

Independent claims 1, and 18-21 (all of the pending independent claims) stand rejected under 35 U.S.C. § 102(e) as allegedly anticipated by Kahle et al. (U.S. Patent Publication 2005/0044434).

A. Independent claim 1, and dependent claims 2-17

With regard to the present invention, independent claim 1 recites "wherein the decode unit is operable to detect for each instruction packet whether the instruction packet defines (i) a plurality of control instructions to be executed sequentially on the first processing channel or (ii) a plurality of instructions comprising at least one data processing instruction to be executed simultaneously on the second execution channel, and to control the first and second channels in dependence on said detection." Anticipation under 35 U.S.C. § 102(e) requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp.*, 713 F. 2d 760, 218 USPQ 781 (Fed. Cir. 1983).

At a minimum, the cited prior art does not disclose (expressly or inherently) the above recited limitation. The examiner asserts, at page 4 of the Office Action, that "it is inherent that instructions are issued to the proper functional unit based on opcode." However, in relying upon the theory of inherency, "the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original).

The examiner has not provided a basis in fact and/or technical reasoning to reasonably support that the limitation "wherein the decode unit is operable to detect for each instruction packet whether the instruction packet defines (i) a plurality of control instructions to be executed

sequentially on the first processing channel or (ii) a plurality of instructions comprising at least one data processing instruction to be executed simultaneously on the second execution channel, and to control the first and second channels in dependence on said detection" necessarily flows from the teachings of Kahle. Kahle appears to assume that instructions are executed serially, and does not expressly or inherently disclose embedding information about possible simultaneous execution in the information packet. This limitation is supported in the Applicant's specification at Figure 2 and paragraph [0027], wherein a value of "0" in the first bit defines an opportunity for simultaneous or parallel execution. Thus, independent claim 1 is not anticipated by Kahle.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as independent claims 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon (claims 2-17) are also patentable. In addition, it is respectfully submitted that the dependent claims 2-17 are patentable based on their own merits by adding novel and non-obvious features to the combination. For example, none of the cited prior art discloses or suggests separating out control code and data path code, due to their different bit widths, and then detecting and distinguishing in order to process these codes separately in order to increase the processing speed and enhance code efficiency.

B. Independent claim 18

With regard to the present invention, independent claim 18 recites in part "decoding an instruction packet to detect whether the instruction packet defines a plurality of control

instructions of equal length or two instructions comprising at least one data instruction, at least one of which is a vector."

At a minimum, the cited prior art does not disclose (expressly or inherently) the above recited limitation. The examiner asserts, at pages 6 and 7 of the Office Action, that "[i]n reading the opcodes the decoder will determine whether the instruction packet defines a plurality of control instructions of equal length or two instructions comprising at least one data instruction, at least one of which is a vector." No prior art is cited, thus this assertion appears to be based on inherency. The examiner has not provided a basis in fact and/or technical reasoning to reasonably support that the limitation "decoding an instruction packet to detect whether the instruction packet defines a plurality of control instructions of equal length or two instructions comprising at least one data instruction, at least one of which is a vector " necessarily flows from the teachings of Kahle. Thus, independent claim 18 is not anticipated by Kahle.

Additionally, claim 18 recites in part "when the instruction packet defines a plurality of instructions comprising at least one data instruction, supplying at least the data instruction to the second processing channel whereby the plurality of instructions are executed simultaneously." This limitation is supported in the Applicant's specification at Figure 2 and paragraph [0027], wherein a value of "0" in the first bit defines an opportunity for simultaneous or parallel execution. The examiner asserts, at Office Action page 7, that the this limitation is disclosed by PowerPC architecture. However, PowerPC architecture such as PPC 970 uses additional hardware to dynamically determine whether some of the instructions within a fetched packet may be co-issued for simultaneous (i.e. order-independent) execution. Such a determination requires at least that the register source and destination addresses of candidate instructions be compared and interlocks applied, that only one memory load or store instruction exists in the

issue group, and that the issue group be truncated (in a program order sense) at each branch instruction. The hardware and power cost of doing this determination is substantial, and the corresponding additional pipelining stages have an adverse impact on performance. In sharp contrast, the claimed 18 recites "the instruction packet defines," and this limitation is supported in the Applicant's specification at Figure 2 and paragraph [0027], wherein a value of "0" in the first bit defines an opportunity for simultaneous or parallel execution.

C. Independent claim 19

Independent claim 19 is a "computer-readable medium" claim that recites in part "wherein the computer-readable medium is adapted to run on a computer such that the first type of instruction packet is executed by a dedicated control processing channel, and the at least one data instruction of the second instruction packet is executed by a dedicated data processing channel, the dedicated control processing channel having a first bit width narrower than the dedicated data processing channel."

The examiner asserts, at Office Action page 8, that the recited limitation is disclosed by Kahle at paragraph [0016]. However, Kahle paragraph [00016] does not disclose the dedicated control processing channel having a first bit width narrower than the dedicated data processing channel. Thus, independent claim 19 is not anticipated by Kahle.

D. Independent claim 20

Independent claim 20 recites "fetching a sequence of instruction packets from a program memory, all of said instruction packets containing a set of designated bits at predetermined bit locations; decoding each instruction packet, said decoding step including reading the values of said designated bits to determine: a) whether the instruction packet defines a plurality of control instructions or a plurality of instructions of which at least one is a data instruction; and b) where

the instruction packet defines a plurality of instructions of which at least one is a data instruction, the nature of each of the instructions selected at least from: a control instruction; a data instruction; and a memory access instruction." The cited prior art (Kahle) does not disclose this limitation, see the discussion above regarding claims 1 and 18.

E. Independent claim 21

Independent claim 21 is "computer-readable medium" claim which recites in part "said instruction packets including at least one indicator bit at a designated bit location within the instruction packet, wherein the computer-readable medium is adapted to run on a computer such that said indication bit is adapted to cooperate with a decode unit of the computer to designate whether: a) the instruction packet defines a plurality of control instructions or a plurality of instructions of which at least one is a data instruction; and b) in the case when there is a plurality of instructions comprising at least one data instruction, the nature of each of the first and second instructions selected from: a control instruction; a data instruction; and a memory access instruction."

The examiner asserts, at Office Action page 10, that the recited limitation is disclosed by Kahle at paragraph [0016]. However, Kahle paragraph [00016] does not disclose the recited indicator bit to designate and define the recited types of instructions. Thus, independent claim 21 is not anticipated by Kahle.

CONCLUSION

For at least the above reasons, all pending claims 1-21 are in condition for allowance. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call the Applicant's' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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